## Open access to low cost photonic integrated circuits prototyping in a generic Silicon Nitride foundry

**David Domenech**<sup>1</sup>, Iñigo Artundo<sup>1</sup>, Bernardo Gargallo<sup>1</sup>, Rocio Baños<sup>1</sup>, Pascual Muñoz<sup>1,2</sup>, Carlos Dominguez<sup>3</sup>

- 1. VLC Photonics S.L., Camino de Vera s/n, 46022 Valencia (SPAIN)
- 2. iTEAM Research Institute, Universitat Politècnica de València, Camino de Vera s/n, 46022 Valencia (SPAIN)
- 3. Institute of Microelectronics of Barcelona, IMB-CNM (CSIC), 08193 Bellaterra (SPAIN) david.domenech@vlcphotonics.com

## **Abstract**

A Silicon Nitride  $(Si_3N_4)$  waveguide platform [1] has been developed with very low propagation losses, low autofluorescence and a high level of integration to realize compact systems at low cost targeted from the visible spectrum to the infrared. Passive components are introduced here with best-in-class performance, including waveguides, splitters, filters, multiplexers and couplers based on optimized ultralow loss  $Si_3N_4$  material as shown in Fig. 1. In order to make efficient use of the fabrication runs and inspired by the cost sharing model that has been in use for ASICs and silicon photonics in the past, access to the fabrication platform is offered through Multi Project Wafer runs (MPW's) [2]. There are two different sizes that users can choose from: M with an area of 5,5 x 5,5 mm², and L with an area of 11 x 5,5 mm² as shown in Fig. 2. The full wafer will be later diced in individual areas and several copies of the chips will be delivered to the users.

## References

- [1] Daldosso, N. *et al.* Comparison among various Si<sub>3</sub>N<sub>4</sub> waveguide geometries grown within a CMOS fabrication pilot line. IEEE J. Lightwave Technol. 22, 1734–1740 (2004)
- [2] M. Smit, X. Leijtens, E. Bente, J. Van der Tol, H. Ambrosius, D. Robbins, M. Wale, N. Grote and M. Schell, "Generic foundry model for InP-based photonics". IET Optoelectron, Vol. 5, pp. 187-194, 2011

## **Figures**

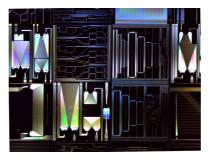


Fig. 1. Multiple components fabricated in a Si<sub>3</sub>N<sub>4</sub> MPW

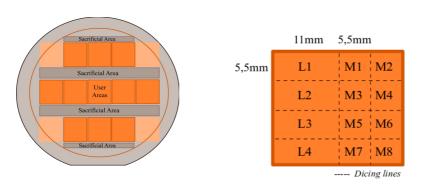


Fig. 2. Wafer plan and reticle division for the CNM MPW run